논리회로 설계 및 실험

8주차

8주차 목표

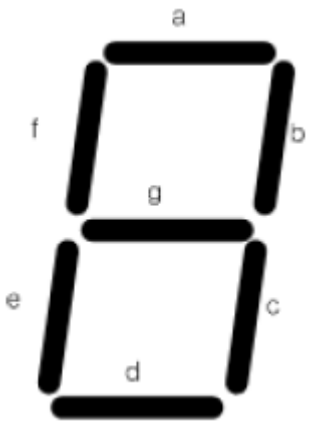
목표

1. 7 Segment의 원리와 사용에 대한 이해

7 Segment의 구성

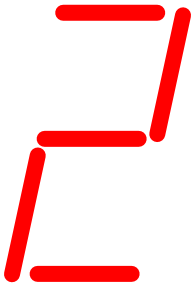
7 Segment

- 7개의 획으로 문자나 숫자 등을 표현할 수 있는 표시장치



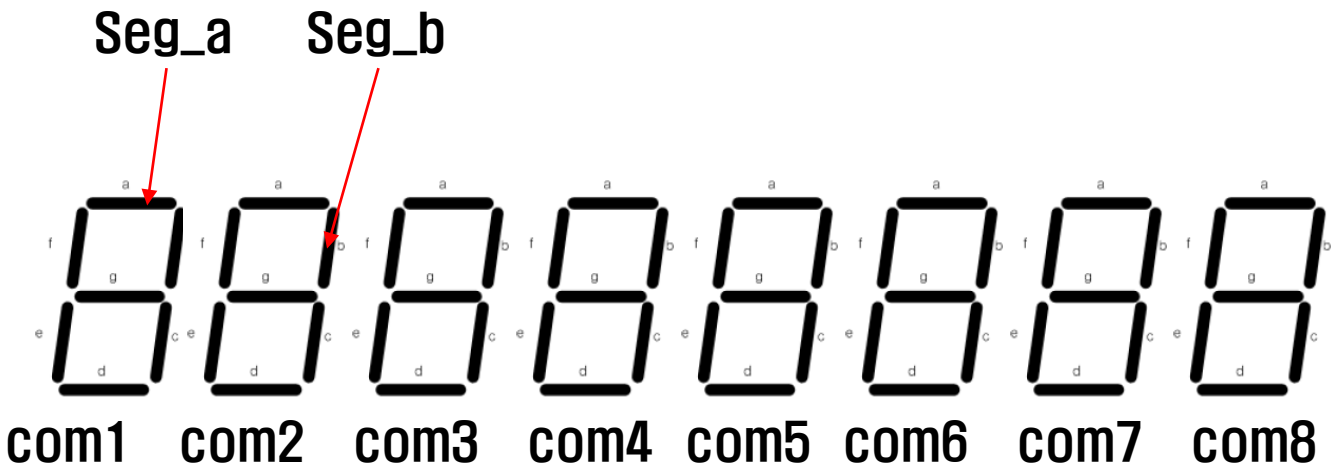
b, c 핀 사용

a, b, d, e, g핀 사용



7 Segment Array

- 다수의 7 Segment를 사용한 표시장치
- Seg_a ~ Seg_g : 각 획을 나타냄
- Seg_com1 ~ Seg_com8 : 각 7 Segment의 자리를 나타냄



7 Segment Array

- Seg_data 는 모두 연결되어 있으며 모든 자리의 Seg_data는 동시에 동작함

com1	com2	com3	com4	com5	com6	com7	com8
0	0	0	0	0	0	0	0

Seg_a	Seg_b	Seg_c	Seg_d	Seg_e	Seg_f	Seg_g	
0	1	1	0	0	0	0	

7 Segment Array

- 각 자리에 서로 다른 데이터를 출력하기 위해서는 아래와 같은 방법을 사용

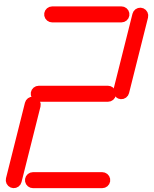
com1 com2 com3 com4 com5 com6 com7 com8

com1	com2	com3	com4	com5	com6	com7	com8
0	1	1	1	1	1	1	1

Seg_a	Seg_b	Seg_c	Seg_d	Seg_e	Seg_f	Seg_g	
0	1	1	0	0	0	0	

7 Segment Array

- 각 자리에 서로 다른 데이터를 출력하기 위해서는 아래와 같은 방법을 사용



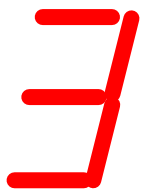
com1 com2 com3 com4 com5 com6 com7 com8

com1	com2	com3	com4	com5	com6	com7	com8
1	0	1	1	1	1	1	1

Seg_a	Seg_b	Seg_c	Seg_d	Seg_e	Seg_f	Seg_g	
1	1	0	1	1	0	1	

7 Segment Array

- 각 자리에 서로 다른 데이터를 출력하기 위해서는 아래와 같은 방법을 사용



com1 com2 com3 com4 com5 com6 com7 com8

com1	com2	com3	com4	com5	com6	com7	com8
1	1	0	1	1	1	1	1

Seg_a	Seg_b	Seg_c	Seg_d	Seg_e	Seg_f	Seg_g	
1	1	1	1	0	0	1	

Clock 사용

① FPGA clock Pin번호 : AB16

```
ERROR:Place:1108 - A clock IOB / BUFGMUX clock component pair have been found
    that are not placed at an optimal clock IOB / BUFGMUX site pair. The clock
    IOB component <clk> is placed at site <AB16>. The corresponding BUFG
    component <clk_BUFGP/BUFG> is placed at site <BUFGMUX_X2Y3>. There is only a
    select set of IOBs that can use the fast path to the Clocker buffer, and they
    are not being used. You may want to analyze why this problem exists and
    correct it. If this sub optimal condition is acceptable for this design, you
    may use the CLOCK_DEDICATED_ROUTE constraint in the .ucf file to demote this
    message to a WARNING and allow your design to continue. However, the use of
    this override is highly discouraged as it may lead to very poor timing
    results. It is recommended that this error condition be corrected in the
    design. A list of all the COMP.PINs used in this clock placement rule is
    listed below. These examples can be used directly in the .ucf file to
    override this clock rule.
    < NET "clk" CLOCK_DEDICATED_ROUTE = FALSE; >

  Phase 4.2  Initial Placement for Architecture Specific Features
  (Checksum:92f031) REAL time: 6 secs

  Total REAL time to Placer completion: 6 secs
  Total CPU  time to Placer completion: 5 secs
ERROR:Pack:1654 - The timing-driven placement phase encountered an error.
```

⇒ clock 사용 시 에러 발생

Clock 사용

① clock을 사용하는 모듈->마우스오른쪽
->Add Source-> 모듈의 .ucf 파일선택

② .ucf파일을 열어
NET “[clock포트이름]" CLOCK_DEDICATED_ROUTE = FALSE; 추가

```
# PlanAhead Generated physical constraints

NET "clk" LOC = AB16;
NET "in" LOC = K2;
NET "out" LOC = K8;
NET "rst" LOC = T4;

NET "clk" CLOCK_DEDICATED_ROUTE = FALSE;
```

Level to Pulse 설계

- clock의 속도가 빠르기 때문에 버튼 입력이 있을 경우 한 번만 동작하도록 설계
- Stadian으로 간단하게 설계가 가능

- Input : clock, reset, input_signal
- Output : output_signal